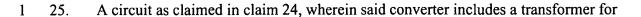
1 <u>CLAIMS</u>

- 2 1. A variable power regulator, comprising:
- a pulse modulator generating a pulse signal having a pulse width; and
- 4 a phase delay array receiving said pulse signal and a frequency selection signal, and
- 5 generating a plurality of phased burst signals, each having a frequency determined by said
- 6 frequency selection signal wherein at least two of said phased burst signals have different start
- 7 times.
- 8 2. A circuit as claimed in claim 1, wherein each said phased burst signal of said plurality of
- 9 phased burst signals regulates a respective load.
- 10 3. A circuit as claimed in claim 1, wherein said pulse modulator includes a variable selector
- 11 for selecting said pulse width.
- 12 4. A circuit as claimed in claim 3, wherein said variable selector comprises a dimmer
  - providing a DC signal, and an oscillator generating a triangular waveform, wherein said pulse
  - width being determined by the intersection of said DC signal and said triangular waveform.
- 15 5. A circuit as claimed in claim 4, wherein said dimmer further comprising a dim selector
  - 16 for setting the DC value of said DC signal, and a polarity selector for determining the section, of
  - 17 said intersection of said DC signal and said triangular waveform, to be used for generating the
  - pulse width of said pulse width modulated signal.
  - 19 6. A circuit as claimed in claim 1, further comprising a frequency selector receiving a
  - 20 reference signal and generating said frequency selection signal based on said reference signal,
  - 21 wherein said phase delay array receiving said frequency selection signal and setting the
  - frequency of said pulse signal to said frequency selection signal.

- 2 timing each said phased burst signal of said plurality of phased burst signals such that at least
- 3 two of said phased burst signals have different start times.
- 4 A circuit as claimed in claim 1, wherein each said phased burst signal has a pulse width 8.
- 5 equal to said pulse width of said pulse signal.
- 6 9. A circuit as claimed in claim 1, wherein said phase delay array includes a phase delay
- 7 generator for generating at least one phase delay value.
- A circuit as claimed in claim 9, wherein said at least one phase delay value is a constant. 10.
- A circuit as claimed in claim 1, wherein said phase delay array includes at least one select 11.
  - signal input for determining the number of said phased burst signals to generate.
  - A circuit as claimed in claim 1, further comprising at least one phase array driver 12.
- 12 13 13 14 receiving at least one said phased burst signal and generating at least one respective power
  - regulating signal for at least one respective load, said power regulating signal having a phase
  - value equal to the phase value of said phased burst signal.
  - A circuit as claimed in claim 12, wherein each phase array driver receives two said 15 13.
  - 16 phased burst signals which are 180° out of phase and generates two respective power regulating
  - 17 signals which are 180° out of phase.
  - 18 14. A circuit as claimed in claim 12, wherein said phase array driver further comprising soft
  - start circuitry generating power to said at least one respective load during a soft start period, 19
  - wherein a soft start period defining a period wherein said at least one load is powered from an 20
  - OFF state to an operationally ON state; and wherein once said load is at least at an operationally 21
  - 22 ON state, power to said load is regulated by said respective phased burst signal during a burst
  - 23 mode period.

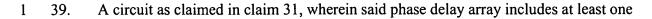
- 1 15. A circuit as claimed in claim 12, wherein said phase array driver further comprising at
- 2 least one comparator for limiting voltage of said at least one load to a predetermined voltage.
- 3 16. A circuit as claimed in claim 14, wherein said phase array driver including at least one
- 4 error amplifier, receiving a feedback from said load during said soft start period, and further,
- 5 receiving feedback from said at least one phased burst signal, wherein said error amplifier
- 6 generates said at least one respective power regulating signal.
- 7 17. A circuit as claimed in claim 12, wherein said phase array driver further comprising at
- 8 least one current or voltage feedback selector for selecting either to regulate current to said at
- 1 least one respective load or regulate the voltage of said at least one respective load.
- 10 18. A circuit as claimed in claim 17, wherein said at least one current or voltage feedback
- selector comprises a multiplexer.
  - 12 19. A circuit as claimed in claim 14, wherein said phase array driver further comprising a
    - selector for selecting either said soft start period or said burst mode period.
  - 14 20. A circuit as claimed in claim 19, wherein said selector comprises a multiplexer.
  - 15 21. A circuit as claimed in claim 12, wherein said phase array driver further comprising a
  - 16 minimum voltage selector to regulate power to said at least one respective load with a selected
  - 17 current or minimum voltage.
  - 18 22. A circuit as claimed in claim 21, wherein said selector comprises a multiplexer.
  - 19 23. A circuit as claimed in claim 12, wherein said phase array driver further comprising a
  - 20 ramp circuit to deliver power to said at least one load.
  - 21 24. A circuit as claimed in claim 12, wherein said phase array driver further comprising a
  - 22 DC/AC converter circuitry for generating an AC signal for at least one respective load.



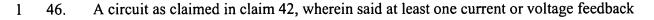
- delivering a high voltage to said load based on said AC signal.
- 3 26. A circuit as claimed in claim 12, wherein said phase array driver further comprising
- 4 protection circuitry for under voltage lock out.
- 5 27. A method for generating phase shifted burst mode signals, comprising the steps of:
- 6 generating a pulse signal having a pulse width;
- 7 generating a frequency selection signal;
- 8 generating a plurality of phased burst signals having a frequency of said frequency
  - selection signal and said pulse width of said pulse signal; and
- delaying at least one of said phased pulse signals to have a different start time than at
- least one other of said phased burst signals.
- 12 28. A method as claimed in claim 27, further comprising the step of:
- regulating power to a plurality of loads using said plurality of said phased burst signals,
- 14 respectively.
- 15 29. A method as claimed in claim 27, further comprising the step of:
- generating a constant phase delay between each said phased burst mode signal.
- 17 30. A method as claimed in claim 28, wherein said step of generating a constant phase delay
- between each said phased burst mode signal comprising the step of dividing the period of said
- 19 frequency selection signal by the number of loads utilized in said plurality of loads to generate a
- value for said constant phase delay.
- 21 31. A phased burst mode dimming system, comprising:
- a pulse width modulator generating a pulse width modulated signal;
- a variable selector for selecting the width of said pulse width modulated signal; and

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- a phase delay array receiving said pulse modulated signal and said frequency selection 1
- 2 signal, and generating a plurality of phased burst signals by generating a phase delay between at
- 3 least two said pulse width modulated signals.
- 4 32. A circuit as claimed in claim 31, wherein said variable selector comprises a dimmer
- providing a DC signal, and an oscillator generating a triangular waveform, wherein said pulse 5
- width being determined by the intersection of said DC signal and said triangular waveform. 6
- 7 A circuit as claimed in claim 32, wherein said dimmer further comprising a dim selector 33.
- 8 for setting the DC value of said DC signal, and a polarity selector for determining the section, of
- 9 said intersection of said DC signal and said triangular waveform, to be used for generating the
- ∬ \*√ 10 pulse width of said pulse width modulated signal.
- T 11 A circuit as claimed in claim 31, further comprising a frequency selector receiving a 34. M
  - reference signal and generating a frequency selection signal, wherein said phase delay array
  - receiving said frequency selection signal and setting the frequency of said pulse signal to said
- 12 13 13 14 frequency selection signal.
  - 15 A circuit as claimed in claim 31, wherein said phase delay array includes a counter for 35.
  - 16 timing each said phased burst signal of said plurality of phased burst signals such that at least
  - 17 two of said phased burst signals have different start times.
  - A circuit as claimed in claim 31, wherein each said phased burst signal has a pulse width 18 36.
  - 19 equal to said pulse width of said pulse signal.
  - A circuit as claimed in claim 31, wherein said phase delay array includes a phase delay 20 37.
  - 21 generator for generating at least one phase delay value.
  - A circuit as claimed in claim 37, wherein said at least one phase delay value is a constant. 22 38.



- 2 select signal input for determining the number of said phased burst signals to generate.
- 3 40. A circuit as claimed in claim 31, further comprising at least one phase array driver
- 4 receiving at least one said phased burst signal and generating at least one respective power
- 5 regulating signal for at least one respective load, said power regulating signal having a phase
- 6 value equal to the phase value of said phased burst signal.
- 7 41. A circuit as claimed in claim 40, wherein each phase array driver receives two said
- 8 phased burst signals which are 180° out of phase and generates two respective power regulating
- 9 signals which are 180° out of phase.
- 10 42. A circuit as claimed in claim 40, wherein said phase array driver further comprising soft
- start circuitry generating power to said at least one respective load during a soft start period,
- wherein a soft start period defining a period wherein said at least one load is powered from an
- OFF state to an operationally ON state; and wherein once said load is at least at an operationally
- ON state, power to said load is regulated by said respective phased burst signal.
- 15 43. A circuit as claimed in claim 40, wherein said phase array driver further comprising a
- 16 comparator for limiting voltage of said at least one load to a predetermined voltage.
- 17 44. A circuit as claimed in claim 42, wherein said phase array driver further comprising at
- least one error amplifier, receiving a feedback from said load during said soft start period, and
- 19 further, receiving feedback from said at least one phased burst signal, wherein said error
- amplifier generates said at least one respective power regulating signal.
- 21 45. A circuit as claimed in claim 40, wherein said phase array driver further comprising at
- least one current or voltage feedback selector for selecting either to regulate current to said at
- 23 least one respective load or regulate the voltage of said at least one respective load.



- 2 selector comprises a multiplexer.
- 3 A circuit as claimed in claim 42, wherein said phase array driver further comprising a 47.
- 4 selector for selecting either said soft start period or said burst mode period.
- A circuit as claimed in claim 42, wherein said at least one burst mode selector comprises 5 48.
- 6 a multiplexer.
- 7 49. A circuit as claimed in claim 40, wherein said phase array driver further comprising a
- minimum voltage selector to regulate power to said at least one respective load with a selected
- current or minimum voltage.
- 50. A circuit as claimed in claim 49, wherein said selector comprises a multiplexer.
- 51. A circuit as claimed in claim 40, wherein said phase array driver further comprising a
- ramp circuit to deliver power to said at least one load.
- 13 52. A circuit as claimed in claim 40, wherein said phase array driver further comprising a
- 14 DC/AC converter circuit generating an AC signal to supply power to at least one respective load.
- 15 53. A circuit as claimed in claim 52, wherein said converter includes a transformer for
- 16 delivering high voltage to said load based on said AC signal.
- 17 54. A circuit as claimed in claim 40, wherein said phase array driver further comprising
- 18 protection circuitry for under voltage lock out.
- 19 55. A circuit as claimed in claim 6, wherein said frequency selector comprises a frequency
- 20 doubler, doubling the frequency of said reference signal, and generating said frequency selection
- 21 signal having a period twice that of said reference signal.
- 22 56. A circuit as claimed in claim 34, wherein said frequency selector comprises a frequency
- 23 doubler, doubling the frequency of said reference signal, and generating said frequency selection

signal having a period twice that of said reference signal.